

IN THE CLAIMS:

Please cancel claim 36 without prejudice or disclaimer.

Please note that all claims that remain pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

D1 Sub G1
31. (Twice amended) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses; and
a plurality of contiguous mesas forming a maze-like structure.

re 32. The storage poly of claim 31, wherein said mesas extend in the X, Y and Z coordinates.

D2 Sub G2
33. (Twice amended) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses;
a plurality of contiguous webs forming a maze-like structure; and
hemispherical-grain polysilicon on top surfaces of at least some of said plurality of contiguous webs.

re 34. The storage poly of claim 31, wherein said webs extend in the X, Y and Z coordinates.

Sub F1 D3
35. (Amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure with recesses formed therein;
a hemispherical-grain polysilicon layer over said storage poly structure; and
a mask over said hemispherical-grain polysilicon layer, said recesses being exposed through said hemispherical-grain polysilicon layer and said mask.

Sub H2 D4
37. (Amended) An intermediate semiconductor memory cell structure, comprising:
a storage poly structure;

low elevation regions of a hemispherical-grain polysilicon layer on said storage poly structure;
recesses formed in said storage poly structure and located laterally between said low elevation
regions of said hemispherical-grain polysilicon layer; and
dielectric material at least lining the recesses.

D4 38. (Amended) A semiconductor memory cell structure, comprising:
a storage poly structure;
regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage
poly structure;
a plurality of recesses extending into said storage poly structure, at least some recesses of said
plurality of recesses being located laterally between said regions of hemispherical-grain
polysilicon; and
and a dielectric layer substantially coating an upper surface of said storage poly structure and
substantially lining each of said plurality of recesses.

re 39. The semiconductor memory cell structure of claim 38, further comprising a cell
poly structure over said dielectric layer.

re 40. The semiconductor memory cell structure of claim 38, wherein said storage poly
structure has a web-like structure.

re 41. The semiconductor memory cell structure of claim 38, wherein at least some of
said plurality of recesses extend into said storage poly structure.

D5 42. (Amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure;
a substantially confluent hemispherical-grain polysilicon layer on said storage poly structure; and
a mask positioned over said substantially confluent hemispherical-grain polysilicon layer,
elevated portions of said hemispherical-grain polysilicon layer being exposed through
said mask.

sub E2 43. (Amended) An intermediate semiconductor capacitor structure, comprising:

a storage poly structure including recesses formed therein;
a hemispherical-grain polysilicon layer on at least portions of said storage poly structure; and
a mask positioned over said hemispherical-grain polysilicon layer and spaced apart from said storage poly structure by said hemispherical-grain polysilicon layer, said recesses in said storage poly structure being exposed through said mask.

sub E3 44. (Amended) An intermediate semiconductor capacitor structure, comprising:

D5 a storage poly structure with recesses formed therein;
a hemispherical-grain polysilicon layer on at least portions of the storage poly structure;
a mask overlying at least portions of said hemispherical-grain polysilicon layer; and
dielectric material lining at least said recesses.

sub H5 45. (Amended) An intermediate semiconductor memory cell structure, comprising:
a storage poly structure with recesses formed therein;
low elevation regions of a hemispherical-grain polysilicon layer on at least portions of the storage poly structure;
a mask overlying at least said low elevation regions of said hemispherical-grain polysilicon layer, said recesses being exposed between said low elevation regions of said hemispherical-grain polysilicon layer and through said mask; and
dielectric material at least lining said recesses.